Project
Algorithm Engineering

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Wednesday 16th April, 2014

Memory

Setup and Projects?

Performance Equation

$$\text{s/cycle} \cdot \text{cycle/Instruction} \cdot \text{Instruction/Program}$$

The ultimate measure of performance is s/Program.

The Power Wall

Higher power consumption

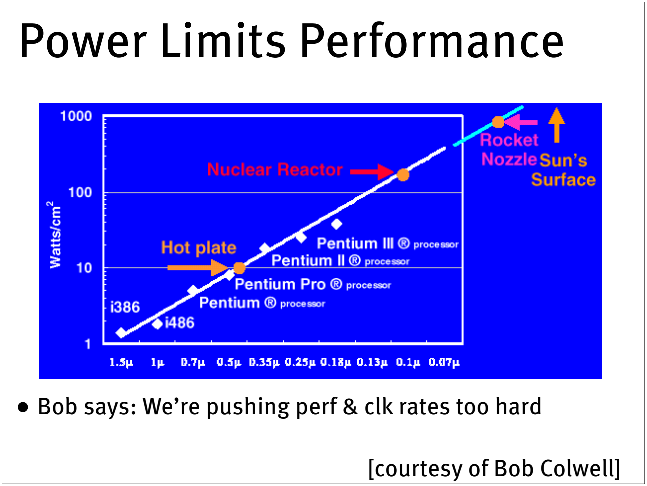

Figure: From [Owe]

The Power Wall (cont.)

Shorter signal propagation

$$1\,\text{GHz, i.e. } 1 \text{ cycle takes } 1\,\text{ns}$$

$$1\,\text{ns} \cdot \underbrace{c_0}_{\approx 300\,\text{Mm/s}} = 0.3\,\text{m}$$

- Power consumption used to be is neglected, because transistors were expensive
- These days power is expensive (GFLOP/W) but since Moore's law still in power transistors are getting cheaper

The Memory Wall

- Growing disparity of speed between CPU and outside memory
- Coined by Wulf and McKee
  William A. Wulf and Sally A. McKee. *Hitting the Memory Wall: Implications of the Obvious*. Tech. rep. Charlottesville, VA, USA, Dec. 1994

$$t_{avg} = p \cdot t_c + (1 - p) \cdot t_m$$

where p is the probability of a cache hit, t_c the time to access on chip memory and t_m is the time to access the outside memory.
t_c and t_m diverge and even though $(1 - p)$ is small we will hit the wall eventually. I.e. the system performance is totally determined by the memory speed.

The Memory Wall (cont.)

- Caches to mitigate memory wall
  (Spatial/Temporal) Locality necessary
- Memory access is crucial for algorithm performance

- Used to be that execution of arithmetic instruction was slow and memory access was fast
- These days a floating-point operation may take few cycles but DRAM access hundreds of cycles

Example

References

John Owens. EEC 171 Parallel Architectures. Introduction / Overview. URL: http://www.nvidia.com/content/cudazone/cudau/courses/ucdavis/lectures/intro.pdf (visited on 04/05/2011) (cit. on p. 5).

William A. Wulf and Sally A. McKee. *Hitting the Memory Wall: Implications of the Obvious*. Tech. rep. Charlottesville, VA, USA, Dec. 1994 (cit. on p. 7).